CLAIMS

What is claimed is:

1. A method comprising:

detecting a write data burst;

determining if at least one memory unit is available to receive the write data burst;

writing the write data burst to the at least one memory unit if the at least one memory unit is available to receive data;

storing a first portion of the write data burst in a buffer, concurrently with activating the at least one memory unit to receive data, if the at least one memory unit is not available to receive data;

writing a second portion of the write data burst to the at least one memory unit when the at least one memory unit is available to receive data; and

writing the first portion of the write data burst from the buffer to the at least one memory unit after writing the second portion of the write data burst.

2. The method of claim 1 wherein the write data burst comprises at least eight data words.

3. The method of claim 1 wherein the first portion write data burst comprises at least one data word.

4. The method of claim 1, wherein the write data burst comprises a write data burst during a processor's burst write mode.

5. The method of claim 1, wherein the method is used in a shared bus architecture.

6. The method of claim 1, wherein the first portion of the write data burst and the second portion of the write data burst are stored in contiguous memory locations.

7. The method of claim 1, wherein the first portion of the write data burst and the second portion of the write data burst are stored in non-contiguous memory locations.

8. The method of claim 1, wherein the at least one memory unit comprises a Synchronous Dynamic Random Access Memory (SDRAM) bank.

9. An apparatus comprising:
a circuit to detect a write data burst to at least one memory unit, to determine if the at least one memory unit is available to receive data, and to write the write data burst to the at least one memory unit if the at least one memory unit is available to receive data;
a buffer communicatively coupled to the circuit to temporarily store a first portion of the write data burst if the at least one memory unit is not available to receive data; and
the circuit to concurrently detect availability of the memory unit, to activate the at least one memory unit to store a second portion of the write data burst, the circuit to further store the first portion of the write data burst from the buffer to the at least one memory

unit after storing the second portion of the write data burst in the at least one memory unit when the at least one memory unit is available to receive data.

10. The apparatus of claim 9, wherein the write data burst comprises at least eight data words.

11. The apparatus of claim 9, wherein the first portion of the write data burst comprises at least one data word.

12. The apparatus of claim 9, wherein the write data burst comprises a sequence of data words output during a processor's burst write mode.

13. The apparatus of claim 9, wherein the apparatus is used in a shared bus architecture.

14. The apparatus of claim 9, wherein the first portion of the write data burst and the second portion of the write data burst are stored in contiguous memory locations.

15. The apparatus of claim 9, wherein the first portion of the write data burst and the second portion of the write data burst are stored in non-contiguous memory locations.

16. The apparatus of claim 9 wherein the at least one memory unit comprises a Synchronous Dynamic Random Access Memory (SDRAM) bank.

17. An apparatus comprising:

means for detecting a write data burst;

means for determining if at least one memory unit is available to receive the write data burst;

means for writing the write data burst to the at least one memory unit if the at least one memory unit is available to receive data;

means for storing a first portion of the write data burst in a buffer, concurrently with activating the at least one memory unit to receive data, if the at least one memory unit is not available to receive data;

means for writing a second portion of the write data burst to the at least one memory unit when the at least one memory unit is available to receive data; and

means for writing the first portion of the write data burst from the buffer to the at least one memory unit after writing the second portion of the write data burst..

18. The apparatus of claim 17, wherein the means for writing the write data burst to the at least one memory unit if the at least one memory unit is available to receive data comprises means for writing at least eight data words in the at least one memory unit during a burst write operation.

19. The apparatus of claim 17, wherein the means for storing a first portion of the write data burst in a buffer concurrently with activating the at least one memory unit to receive data comprises means for storing at least one data word in the buffer.

20. A computer system comprising:

a memory controller to detect a write data burst to at least one memory unit, to determine if the at least one memory unit is available to receive data, and to write the write data burst to the at least one memory unit if the at least one memory unit is available to receive data;

a buffer communicatively coupled to the memory controller to temporarily store a first portion of the write data burst if the at least one memory unit is not available to receive data; and

the memory controller to concurrently detect availability of the memory unit, to activate the at least one memory unit to store a second portion of the write data burst, the circuit to further store the first portion of the write data burst from the buffer to the at least one memory unit after storing the second portion of the write data burst in the at least one memory unit when the at least one memory unit is available to receive data.

21. The computer system of claim 20, wherein the write data burst comprises a write data burst output during a processor's burst write mode

22. The computer system of claim 20, further comprising the buffer to store at least one data word.

23. The computer system of claim 20, further comprising the computer system using a shared bus architecture.

24. An article of manufacture comprising:

a machine-accessible medium including instructions that when executed by a machine, causes said machine to perform operations comprising:

detecting a write data burst;

determining if at least one memory unit is available to receive the write data burst;

writing the write data burst to the at least one memory unit if the at least one memory unit is available to receive data;

storing a first portion of the write data burst in a buffer, concurrently with activating the at least one memory unit to receive data, if the at least one memory unit is not available to receive data;

writing a second portion of the write data burst to the at least one memory unit when the at least one memory unit is available to receive data; and

writing the first portion of the write data burst from the buffer to the at least one memory unit after writing the second portion of the write data burst.

25. The article of manufacture of claim 24, wherein said instructions for writing the write data burst to the at least one memory unit if the at least one memory unit is available to receive data, includes further instructions to write at least eight data words to the at least one memory unit during a burst write operation.

26. The article of manufacture of claim 24, wherein said instructions for storing a first portion of the write data burst in a buffer, concurrently with activating the at least one memory unit to receive data, includes further instructions to store at least one data word in the buffer.

27. The article of manufacture of claim 24, wherein said article of manufacture is used in a shared bus architecture.

28. An apparatus comprising:

a register to store address information of a memory unit that is available to receive data;

a comparator to compare address information from the register with address information of a memory unit that is being accessed, the output of the comparator to drive a finite state machine;

a buffer, communicatively coupled to the FSM to temporarily store a first portion of a write data burst if memory is not available to receive data;

the FSM to enable the memory being accessed if the memory is not available to receive data, the memory to store a second portion of the write data burst when the memory being accessed is available to receive data; and

the finite state machine to store the first portion of the write data burst from the buffer to the memory being accessed.

29. The apparatus of claim 28, wherein the write data burst comprises at least eight data words.

30. The apparatus of claim 28, wherein the first portion of the write data burst comprises at least one data word.

31. The apparatus of claim 28, wherein the memory comprises Synchronous Dynamic Random Access Memory (SDRAM).